

Appl. No. 10/044,155
Amdt. Dated April 7, 2005
Reply to Office action of January 10, 2005

Remarks/Arguments

Claims 1-7, 9, 11, 13 and 15-17 (including new claims 15-17) remain in this application.

The examiner has objected to the specification as failing to provide proper antecedent basis for the claimed subject matter in claims 8, 10, 12 and 14.

The examiner has rejected claims 1-14 under 35 USC 102(e) as being anticipated by *Dervisoglu, et al.*, United States Published Patent Application 2003/0131327.

In view of the above amendments and these remarks, reconsideration of the above noted rejections and objections is respectfully requested.

Specification Objections:

Due to the above amendments, Applicant respectfully requests withdrawal of the objection to the specification as failing to provide proper antecedent basis for the claimed subject matter in claims 8, 10, 12 and 14. Claims 8, 10, 12 and 14 have been canceled by the above amendments. Applicant respectfully submits that these amendments cure the grounds for the objection to the specification.

Rejections under 35 USC 102(e):

Applicant respectfully traverses the rejection of **claims 1-14** under 35 USC 102(e) as being anticipated by *Dervisoglu, et al.* The independent claims are **1, 2, 4 and 5**. Independent **claim 1** calls for “test signals” generated at “test points in the IC” and routing the test signals through a hierarchy of multiplexers to “output locations” to which selected portions of the test signals, themselves, are supplied. Similarly, independent **claims 2 and 4** call for passing “test signals,” themselves, from “test points” through various multiplexers to “output locations.” Additionally, independent **claim 5** calls for passing “test signals” through various “selecting means” to “means for outputting selected ones of the test signals,” themselves. Applicant respectfully submits that *Dervisoglu, et al.* does not teach or suggest

passing or routing test signals, themselves, to “output locations” or “outputting means.”

Dervisoglu, et al. describes capturing test data, serializing the data, and outputting the data in serial at a serial output port on an IC. (paragraph [0045]) In other words, captured data is created from the generated “test signals” in *Dervisoglu, et al.* at the level of the boundary-scan registers 124. It is the captured data created from the test signals, not the test signals themselves, that is transferred through the socket access ports (220, 221, 235 and 236) upward in the hierarchical structure to the chip access port (205). Therefore the test signals in *Dervisoglu, et al.* are not passed or routed to the output location or means (i.e. the chip access port), as called for in the present claims.

Unlike the device in *Dervisoglu, et al.*, the presently claimed invention can present actual live, active signals at the output locations or outputting means. Having live information is extremely useful because some test signals may experience a glitch, and the glitch can be the root cause of an error being debugged in the IC. It is not possible, however, to observe the actual signals at the output locations of the IC using *Dervisoglu's* method, because *Dervisoglu, et al.* produces only captured data, rather than the actual signals.

Additionally, the output locations and/or outputting means called for in claims 1, 2, 4 and 5 are plural, which is necessary in order to produce more than one actual live, active test signal from the IC, since the “test signals” element in these claims is also plural. *Dervisoglu, et al.*, on the other hand, discloses that the chip access port (CAP), the test access port (TAP) and the socket access ports (SAP) comply with IEEE standard 1149.1 (paragraphs [0019], [0043], [0048], [0050] and [0053]), which calls for serializing output data. Additionally, *Dervisoglu, et al.* states at [0057] that “Preferably, both the boundary-scan cells (or registers) 240 and the instruction register of the chip access port 205 are loaded and unloaded using serial access (i.e., scan) of their contents, via the Test Data Input (TDI) signal pin and Test Data Output (TDO) signal pin, respectively.” *Dervisoglu, et al.*, therefore, teaches

outputting serialized data at a single output (i.e. the Test Data Output (TDO) signal pin). It is not possible to produce plural actual live, active test signals using only a single output.

Applicant respectfully submits, therefore, that independent claims 1, 2, 4 and 5 are not anticipated by, are not obvious from, and are patentable over *Dervisoglu, et al.*, since the reference does not teach or fairly suggest passing or routing plural test signals to plural output locations or outputting means as claimed. Additionally; since claims 7 and 15 dependent from independent claim 1, claims 3, 9 and 16 depend from independent claim 2, claim 11 depends from independent claim 4, and claims 6, 13 and 17 depend from independent claim 5; these claims also are not anticipated by, are not obvious from, and are patentable over *Dervisoglu, et al.* for the same reasons.

Additionally, independent claim 4 further states that "a portion of the test signals are measured" at the output locations. The device in *Dervisoglu, et al.*, however, cannot produce "measurable" test signals at its output point, since *Dervisoglu* does not output the actual test signals, but only outputs the captured data, as described above. There is no measurement that can be made once the data has already been captured. Applicant respectfully submits, therefore, that independent claim 4 is not anticipated by, is not obvious from, and is patentable over *Dervisoglu, et al.*, since the reference does not teach or fairly suggest that the test signals passed or routed to the output locations or outputting means are measured as claimed. Additionally, since claim 11 depends from independent claim 4; this claim also is not anticipated by, is not obvious from, and is patentable over *Dervisoglu, et al.* for the same reasons.

New Claims:

New dependent claims 15-17 have been added to the Application. Applicant respectfully submits that these new claims do not add new matter. Specifically, new dependent claims 15-17 depend from independent claims 1, 2 and 5, respectively, and include the above described measurement limitation. Applicant respectfully

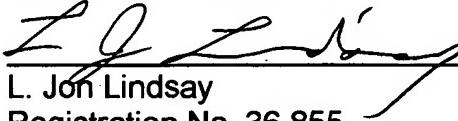
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submits, therefore, that new **claims 15-17** are not anticipated by, are not obvious from, and are patentable over *Dervisoglu, et al.* for the same reasons that independent claims 1, 2 and 5 are not anticipated by, are not obvious from, and are patentable over *Dervisoglu, et al.* Applicant respectfully further submits that new **claims 15-17** are not anticipated by, are not obvious from, and are patentable over *Dervisoglu, et al.* for the same reasons that claims 4 and 11 are not anticipated by, are not obvious from, and are patentable over *Dervisoglu, et al.*

For the reasons specifically discussed above, and others, it is believed that pending claims 1-7, 9, 11, 13 and 15-17 define patentable subject matter. Reconsideration of the previous rejections as they might apply to the pending claims is therefore respectfully requested. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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